eSi-Peripheral Map

1 Contents

2 Overview

The eSi-Peripheral Map core is an APB peripheral that provides a description of each of the other peripherals connected to the APB bus. It allows a program to determine at run-time where each of the peripherals exist in the CPUs address space and what resources they are using. The eSi-Peripheral Map core provides this information via a table, with each peripheral having an entry in the table. Each entry in the table contains:

- 16-bit vendor identifier
- 16-bit peripheral identifier
- 16-bit peripheral revision number
- Base address and address map size for each peripheral
- Interrupt number, if used
- DMA channel, if used
- Peripheral configuration information, if applicable

3 Hardware Interface

Module Name	cpu_apb_peripheral_map
HDL	Verilog
Technology	Generic
Source Files	cpu_apb_peripheral_map.v

Port	Direction	Width	Description
pclk	Input	1	APB clock
presetn	Input	1	APB reset, active-low
paddr	Input	Variable	APB address
psel	Input	1	APB slave select
penable	Input	1	APB enable
pwrite	Input	1	APB write
pwdata	Input	BITS	APB write data
pready	Output	1	APB ready
prdata	Output	BITS	APB read data
pslverr	Output	1	APB slave error

Table 1: I/O Ports

For complete details of the APB signals, please refer to the AMBA 3 APB Protocol v1.0 Specification available at:

http://www.arm.com/products/system-ip/amba/amba-open-specifications.php

4 Software Interface

4.1 Register Map

The peripheral map table is implemented as an array of read-only registers. The number of registers implement will correspond to the number of peripherals connected to the APB. Table 2: Register Map details the address offset for each field within each table entry, where N is the peripheral number. The table is terminated by an entry that contains zeros in each field. An example register map is given in section 5 Example Register Map on page 5.

Register	Address offset	Access	Description
vendor_id[N]	0x20*N+0x00	R	Vendor identifier
device_id[N]	0x20*N+0x04	R	Device identifier
revision[N]	0x20*N+0x08	R	Revision number
base_address[N]	0x20*N+0x0c	R	Base address
size[N]	0x20*N+0x10	R	Address space size
irq[N]	0x20*N+0x14	R	IRQ number
dma[N]	0x20*N+0x18	R	DMA channel
config[N]	0x20*N+0x1c	R	Peripheral configuration information

Table 2: Register Map

4.1.1 Vendor Identifier

The vendor identifier is a 16-bit unsigned number that identifies the peripheral vendor. Vendor identifiers are the same as manufacturer identifiers as described in the eSi-RISC Architecture Manual.

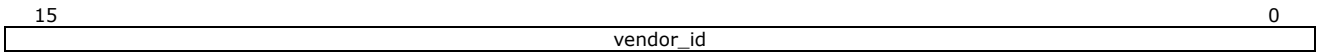

Figure 1: Format of the `vendor_id` register

4.1.2 Device Identifier

The device identifier is a 16-bit unsigned number that identifies the function of a peripheral. Different vendors may use the same identifier for different peripherals. The device identifiers for the eSi-Cores are given in Table 3: eSi-Core Device Identifiers.

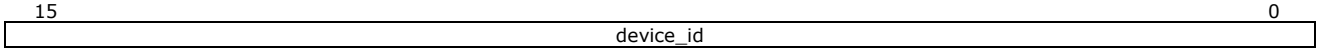

Figure 2: Format of the `device_id` register

Vendor ID	Peripheral ID	Peripheral
0x0006	0x0001	eSi-UART
0x0006	0x0002	eSi-GPIO
0x0006	0x0003	eSi-Timer
0x0006	0x0004	eSi-Watchdog
0x0006	0x0005	eSi-SPI
0x0006	0x0006	eSi-EMAC
0x0006	0x0007	eSi-PS/2
0x0006	0x0008	eSi-LCD
0x0006	0x0009	eSi-I2C
0x0006	0x000b	eSi-USB

0x0006	0x000d	eSi-Multichannel Timer
0x0006	0x000e	eSi-PWM
0x0006	0x000f	eSi-Peripheral Map
0x0006	0x0010	eSi-SWP
0x0006	0x0011	eSi-TRNG
0x0006	0x0012	eSi-AES
0x0006	0x0013	eSi-DES
0x0006	0x0014	eSi-RTC
0x0006	0x0015	eSi-APB-SHA-256
0x0006	0x0016	eSi-APB-SHA-512
0x0006	0x0017	eSi-APB-ECC-Lite
0x0006	0x0018	eSi-APB-ECC-Micro
0x0006	0x0019	eSi-APB-ECDSA
0x0006	0x001a	eSi-Reset
0x0006	0x001b	eSi-PLL Control
0x0006	0x001c	eSi-SPDIF RX
0x0006	0x001d	eSi-SPDIF TX
0x0006	0x1001	eSi-DMA
0x0006	0x1004	eSi-Single Port RAM
0x0006	0x1005	eSi-SMI (Cfg)
0x0006	0x1006	eSi-SIM (Mem)
0x0006	0x1007	eSi-CPU to CPU Interrupt
0x0006	0x1008	eSi-SHA256
0x0006	0x1009	eSi-TSMC Flash (Mem)
0x0006	0x100a	eSi-TSMC Flash (Cfg)
0x0006	0x100b	eSi-CRC
0x0006	0x100c	eSi-Dual Port RAM
0x0006	0x100d	eSi-I2S
0x0006	0x100e	eSi-SPI Flash (Cfg)
0x0006	0x100f	eSi-SPI Flash (Mem)
0x0006	0x1010	eSi-AHB-to-AHB Bridge
0x0006	0x1011	eSi-AHB Triple Port RAM
0x0006	0x1012	eSi-AHB-to-AXI Bridge
0x0006	0x1013	eSi-SG-DMA
0x0006	0x1014	eSi-AHB Single Port RAM
0x0006	0x1015	eSi-FIFO
0x0006	0x1017	eSi-TSMC Flash (Info)
0x0006	0x1018	eSi-AHB AES
0x0006	0x1019	eSi-Delta Sigma
0x0006	0x101a	eSi-LCD

Table 3: eSi-Core Device Identifiers

4.1.3 Revision

The revision number is a 16-bit unsigned number that identifies the hardware revision of a peripheral.

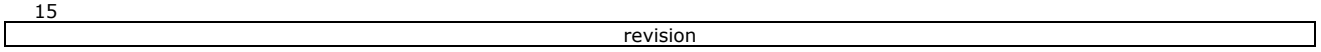

Figure 3: Format of the `revision` register

4.1.4 Base Address

The base address register specifies the base address of the peripherals address space.

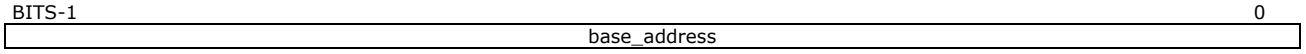

Figure 4: Format of the `base_address` register

4.1.5 Size

The size register specifies the size of the peripherals address space.

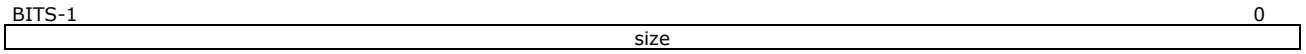

Figure 5: Format of the `size` register

4.1.6 IRQ

The IRQ register specifies the interrupt line the peripheral is connected to the CPU via. A value of -1 indicates that the peripheral either does not have an interrupt output or that the interrupt is not connected.

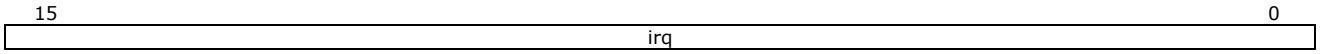

Figure 6: Format of the `irq` register

4.1.7 DMA

The DMA register specifies the DMA channel that the peripheral uses. A value of -1 indicates that the peripheral either does not support DMA or is not connected to a DMA controller.

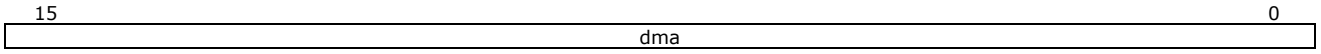

Figure 7: Format of the `dma` register

4.1.8 Config

The Config register provides peripheral specific configuration information. The format of this register varies for each peripheral.

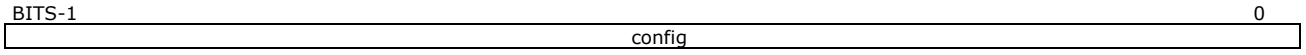

Figure 8: Format of the `config` register

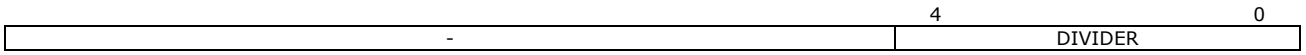

Figure 9: Format of the `config` register for the eSi-AHB to APB Bridge Peripheral

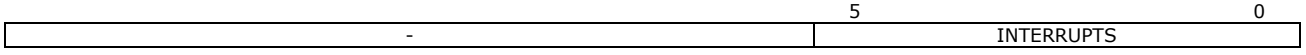

Figure 10: Format of the `config` register for the eSi-CPU-to-CPU Interrupt Peripheral

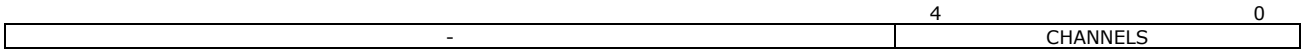

Figure 11: Format of the `config` register for the eSi-DMA Peripheral

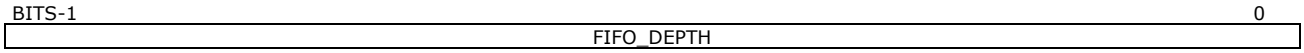

Figure 12: Format of the `config` register for the eSi-FIFO Peripheral

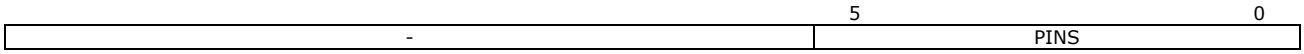

Figure 13: Format of the `config` register for the eSi-GPIO Peripheral

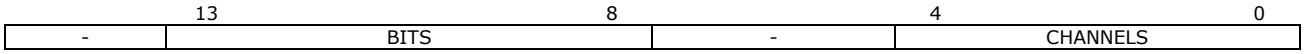

Figure 14: Format of the `config` register for the eSi-Multichannel Timer Peripheral

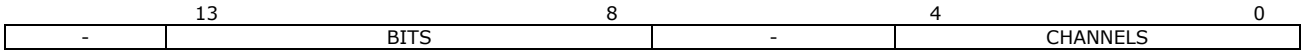

Figure 15: Format of the `config` register for the eSi-PWM Peripheral

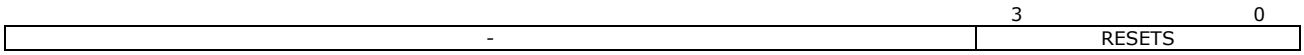

Figure 16: Format of the `config` register for the eSi-Reset Peripheral

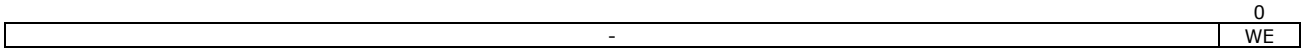

Figure 17: Format of the `config` register for the eSi-SHA-256 Peripheral

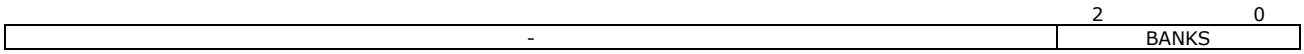

Figure 18: Format of the `config` register for the eSi-SMI Peripheral

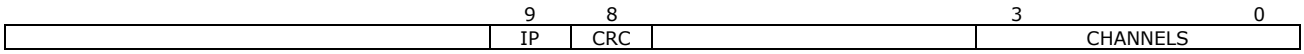

Figure 19: Format of the `config` register for the eSi-SG-DMA Peripheral

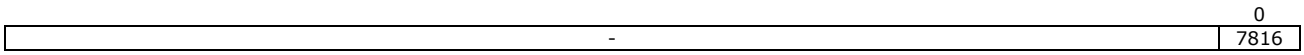

Figure 20: Format of the `config` register for the eSi-UART Peripheral

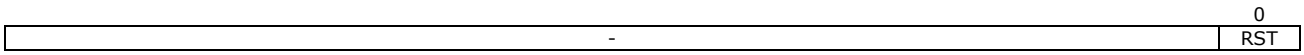

Figure 21: Format of the `config` register for the eSi-Watchdog Peripheral

5 Example Register Map

Table 4 shows one possible register map for a small 16-bit SoC containing a UART and GPIO.

Address offset	Access	Register Value	Description
0x00	R	0x0006	Vendor identifier (EnSilica)
0x04	R	0x0001	Device identifier (UART)
0x08	R	0x0001	Revision number
0x0c	R	0x8000	Base address
0x10	R	0x0100	Address space size
0x14	R	0x0000	IRQ number (0)
0x18	R	0xffff	DMA channel (No DMA)
0x1c	R	0x0003	Indicates 3 DMA channels
0x20	R	0x0006	Vendor identifier (EnSilica)
0x24	R	0x0002	Device identifier (GPIO)
0x28	R	0x0001	Revision number
0x2c	R	0x8100	Base address
0x30	R	0x0100	Address space size
0x34	R	0xffff	IRQ number (No IRQ)
0x38	R	0xffff	DMA channel (No DMA)
0x3c	R	0x0010	Indicates 16 GPIO pins
0x40	R	0x0000	Peripheral Map Terminator
0x44	R	0x0000	
0x48	R	0x0000	
0x4c	R	0x0000	
0x40	R	0x0000	
0x44	R	0x0000	
0x48	R	0x0000	
0x4c	R	0x0000	

Table 4: Example Register Map

6 Revision History

Hardware Revision	Software Release	Description
1	1.0.0	Initial release
2	2.4.0	Added `config` register
2	2.8.11	Add details of UART `config` register
3	3.2.4	Add details of Watchdog `config` register
4	4.1.9	Add details of TSMC Flash `config` register

Table 5: Revision History

