eSi-RISC

PROCESSOR IP

eSi-PS/2

1 Contents

2 Overview

The eSi-PS/2 core can be used as a PS/2 host interface to communicate with devices such as keyboards and mice. It supports the following features:

- Bi-directional communication (device-to-host and host-to-device).
- Parity bit checking and generation.
- Configurable FIFO size.
- AMBA 3 APB slave interface.
- DMA flow-control interface.

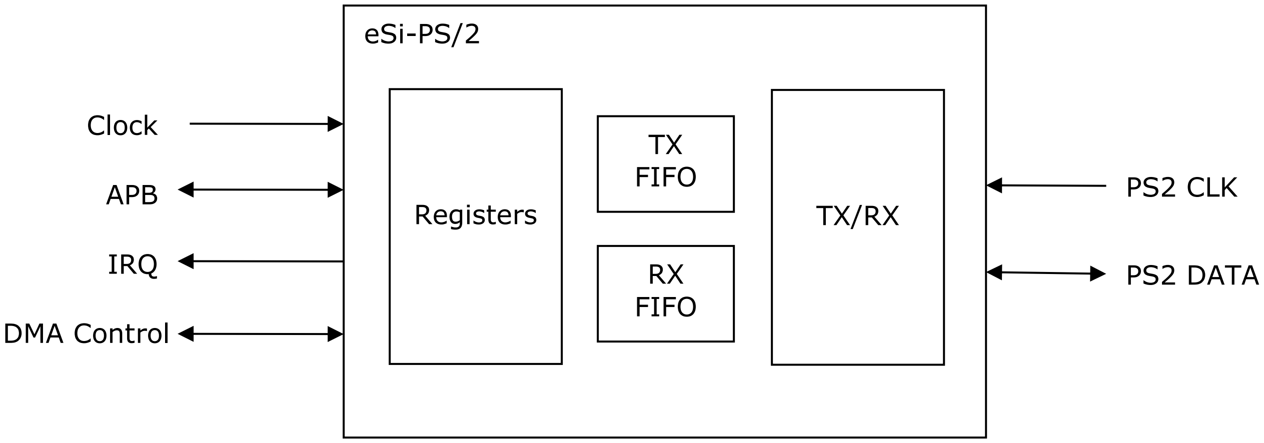

Figure 1: eSi-PS/2

3 Hardware Interface

Module Name	cpu_apb_ps2
HDL	Verilog
Technology	Generic
Source Files	cpu_apb_ps2.v, cpu_fifo.v, cpu_peripheral_flow_control.v

Port	Direction	Width	Description
clk	Input	1	Clock used for data transmission and reception. This clock must be enabled when cactive is asserted.
pclk	Input	1	APB clock
presetn	Input	1	APB reset, active-low
paddr	Input	8	APB address
psel	Input	1	APB slave select
penable	Input	1	APB enable
pwrite	Input	1	APB write
pdebug	Input	1	APB noninvasive debug read
pwdata	Input	16	APB write data
ps2_clk_in	Input	1	PS/2 received clock
ps2_data_in	Input	1	PS/2 received data
tx_ack	Input	1	Acknowledges tx_ready after transfer complete
rx_ack	Input	1	Acknowledges rx_ready after transfer complete
cactive	Output	1	Clock active
pready	Output	1	APB ready
prdata	Output	16	APB read data
pslverr	Output	1	APB slave error
interrupt_n	Output	1	Interrupt request, active-low
ps2_clk_out	Output	1	PS/2 transmit clock
ps2_data_out	Output	1	PS/2 transmit data
tx_ready	Output	1	Indicates device can accept new data
rx_ready	Output	1	Indicates device has data to be read

Table 1: I/O Ports

For complete details of the APB signals, please refer to the AMBA 3 APB Protocol v1.0 Specification available at:

http://www.arm.com/products/system-ip/amba/amba-open-specifications.php

The PS/2 interface module does not include internal synchronizing flip-flops. These should be implemented externally for the ps2_clk and ps2_data ports if the transmitting clock domain is asynchronous to clk.

4 Software Interface

4.1 Register Map

Register	Address offset	Access	Description
tx_data	0x00	W	Transmit register
rx_data	0x04	R	Receive register
status	0x08	R/W	Status register
control	0x0c	R/W	Control register
cycles_per_bit	0x10	R/W	Cycles per bit register

Table 2: Register Map

4.1.1 Transmit Register

Data to be transmitted over the PS/2 interface should be written to the lower 8 bits of the transmit register. The transmit data register should not be written to while the TXF bit in the status register is set, otherwise data loss may occur.

	7	0
	TX	

Figure 2: Format of the tx register

4.1.2 Receive Register

Data that is received over the PS/2 interface and stored in the RX FIFO can be read in the lower 8 bits of the receive register. A read from the received data register will remove the data from the RX FIFO, unless pdebug is high. Setting pdebug high allows a debugger to display the first element in the RX FIFO, without affecting the program being debugged.

	7	0
	RX	

Figure 3: Format of the rx register

4.1.3 Status Register

The status register contains a selection of flags that indicate the current status of the PS/2 interface. To clear a bit in the status register, write a 1 to it. Writing 0 will leave it unchanged.

	7	6	5	4	3	2	1	0
-	PE	FE	RXO	RXF	RXE	TXO	TXF	TXE

Figure 4: Format of the status register

Register	Values	Description
TXE	0 - Not empty 1 - Empty	Transmit buffer empty
TXF	0 - Not full 1 - Full	Transmit buffer full
TXO	0 - No overflow 1 - Overflow	Transmit buffer overflow
RXE	0 - Not empty	Receive buffer empty

	1 - Empty	
RXF	0 - Not full 1 - Full	Receive buffer full
RXO	0 - No overflow 1 - Overflow	Receive buffer overflow
FE	0 - No error 1 - Framing error	Framing error
PE	0 - No error 1 - Parity error	Parity error

Table 3: Fields of the `status` register

4.1.4 Control Register

The control register contains a selection of flags that control the operation of the PS/2 interface.

	2	1	0
-	RXIE	TXIE	E

Figure 5: Format of the `control` register

Register	Values	Description
E	0 - Disabled 1 - Enabled	Enables the PS/2 interface. When disabled, data will not be received or transmitted
TXIE	0 - Disabled 1 - Enabled	Transmit interrupt enable
RXIE	0 - Disabled 1 - Enabled	Receive interrupt enable

Table 4: Fields of the `control` register

4.1.5 Cycles Per Bit Register

The cycles per bit register is a 16-bit that specifies how many cycles of the clock, `clk`, corresponds to one bit period, assuming a PS/2 clock rate of 30kHz. The clock is always driven by the device, so this value is only used to determine how long to pull the clock low when requesting to transmit.

15	0

Figure 6: Format of the `cycles_per_bit` register

4.2 Interrupts

The PS/2 interface supports the following interrupts.

- Transmit interrupt
- Receive interrupt

The transmit interrupt will be raised when the transmit buffer is empty and the `TXIE` flag in the `control` register is set to 1. This indicates that the transmitter has no data to transmit.

The receive interrupt will be raised when the receiver buffer is not empty and the `RXIE` flag in the control register is set to 1. This indicates that the receiver has received some data.

5 Revision History

Hardware Revision	Software Release	Description
1	1.0.0	Initial release
2	2.3.2	Added `tx_ack` and `rx_ack` ports.

Table 5: Revision History