eSi-Multichannel Timer

1 Contents

2 Overview

The eSi-Multichannel Timer is a simple multichannel timer. It has the following features:

- Configurable number of channels.
- Configurable counter width.
- Single-shot or continuous mode.
- Programmable automatic disable during debug.
- AMBA 3 APB slave interface.

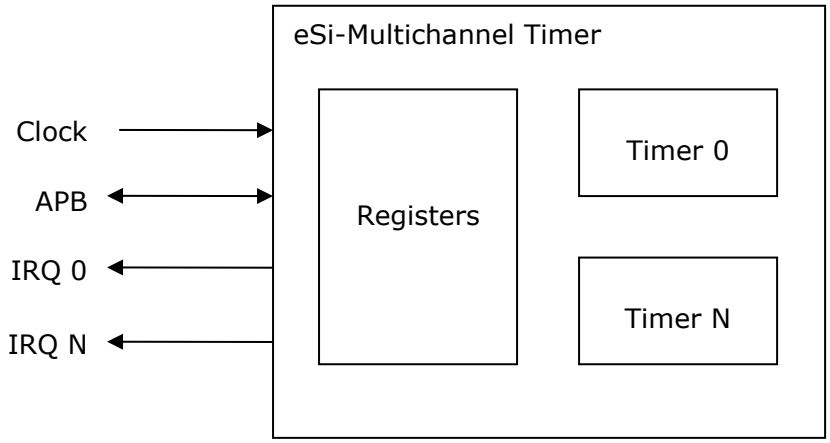


Figure 1: eSi-Multichannel Timer

3 Hardware Interface

Module Name	cpu_apb_multichannel_timer
HDL	Verilog
Technology	Generic
Source Files	cpu_apb_multichannel_timer.v

Port	Type	Description
bits	Integer	Specifies the number of bits in the counters
channels	Integer	Specifies the number of timer channels
apb_data_width	Integer	Width of APB data bus
apb_address_width	Integer	Width of APB address bus

Table 1: Parameters

Port	Direction	Width	Description
clk	Input	1	Clock used for counters. This must be active when cactive is asserted. It must be synchronous to pclk, although can be at a lower frequency.
pclk	Input	1	APB clock
presetn	Input	1	APB reset, active-low
paddr	Input	apb_address_width	APB address (only 8 LSBs are used)
psel	Input	1	APB slave select
penable	Input	1	APB enable
pwrite	Input	1	APB write
pwdata	Input	apb_data_width	APB write data
debug_active	Input	1	Indicates when debugger is active
cactive	Output	1	Indicates clk should be active
pready	Output	1	APB ready
prdata	Output	apb_data_width	APB read data
pslverr	Output	1	APB slave error
interrupt_n	Output	channels	Interrupt request, active-low

Table 2: I/O Ports

For complete details of the APB signals, please refer to the AMBA 3 APB Protocol v1.0 Specification available at:

http://www.arm.com/products/system-ip/amba/amba-open-specifications.php

4 Software Interface

4.1 Register Map

Register	Address offset	Access	Description
counter[N]	0x10*N+0x00	R/W	Counter register for channel N
wrap_comparator[N]	0x10*N+0x04	R/W	Wrap comparator for channel N
status[N]	0x10*N+0x08	R/W	Status register for channel N
control[N]	0x10*N+0x0c	R/W	Control register for channel N

Table 3: Register Map

4.1.1 Counter

Each channel has its own up counter. The bit-width of the counter is specified by the `bits` parameter. When enabled, (`control.E` equals 1), the counter will increment by 1 on every positive edge of `clk`. When the counter contains the same value as in the corresponding wrap comparator register, the counter will be reset to 0. The counter therefore counts in the range [0, `wrap_comparator`].

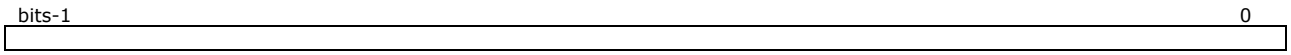
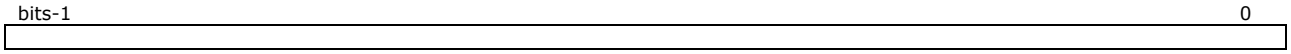


Figure 2: Format of the `counter` register

4.1.2 Wrap Comparator

Each timer channel has its own wrap comparator register. The wrap comparator register contains the value after which the corresponding counter will wrap to 0.



4.1.3 Figure 3: Format of the `wrap_comparator` register

4.1.4 Status Register

Each timer channel has its own status register. Each status register contains a selection of flags that indicate the current status of the corresponding timer channel. To clear a bit in the status register, write a 1 to it. Writing 0 will leave it unchanged.

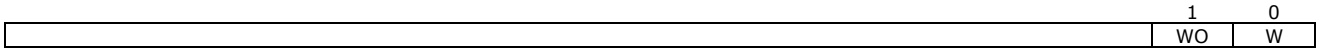


Figure 4: Format of the `status` register

Register	Values	Description
W	0 - No wrap 1 – Wrapped	Wrapped flag. Indicates whether the counter has wrapped
WO	0 - No wrap overflow 1 - Wrap overflow	Wrapped overflow flag. Indicates if the `W` flag was set when the counter wrapped

Table 4: Fields of the `status` register

4.1.5 Control Register

Each timer channel has its own control register. Each control register contains a selection of flags that control the operation of the corresponding timer channel.

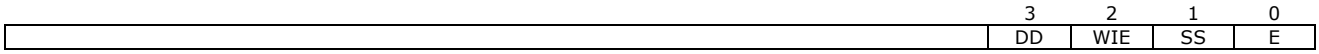


Figure 5: Format of the `control` register

Register	Values	Description
`E`	0 – Disabled 1 – Enabled	Enables the counter
`SS`	0 – Continuous 1 – Single-shot	Single-shot mode
`WIE`	0 – Disabled 1 – Enabled	Wrap interrupt enable
`DD`	0 – Enable during debug 1 – Disable during debug	Disable counter when debugger is active

Table 5: Fields of the `control` register

4.2 Interrupts

The timer supports a per-channel wrap interrupt. The wrap interrupt will be raised when the corresponding counter wraps to 0 and the `WIE` flag in the channel's `control` register is set to 1. The wrap interrupt can be acknowledged by writing a 1 to the corresponding `status.W` flag.

5 Revision History

Hardware Revision	Software Release	Description
1	2.2.0	Initial release
2	2.4.0	Remove `pclk_cactive`. Rename `clk_cactive` to `cactive`.
3	6.0.2	Added `debug_active` input. Added `control.DD` field.

Table 6: Revision History

