eSi-I2S

1 Contents

2 Overview

The eSi-I2S core can be used to transmit and receive audio data via the I²S protocol. It supports the following features:

- Supports simultaneous transmit and receive with independent clocks.
- Programmable support for 8, 16, 20, 24 or 32-bit data.
- Transmit and receive FIFOs with a configurable depth.
- AHB 3 AHB-lite slave interface.
- DMA flow-control interface.

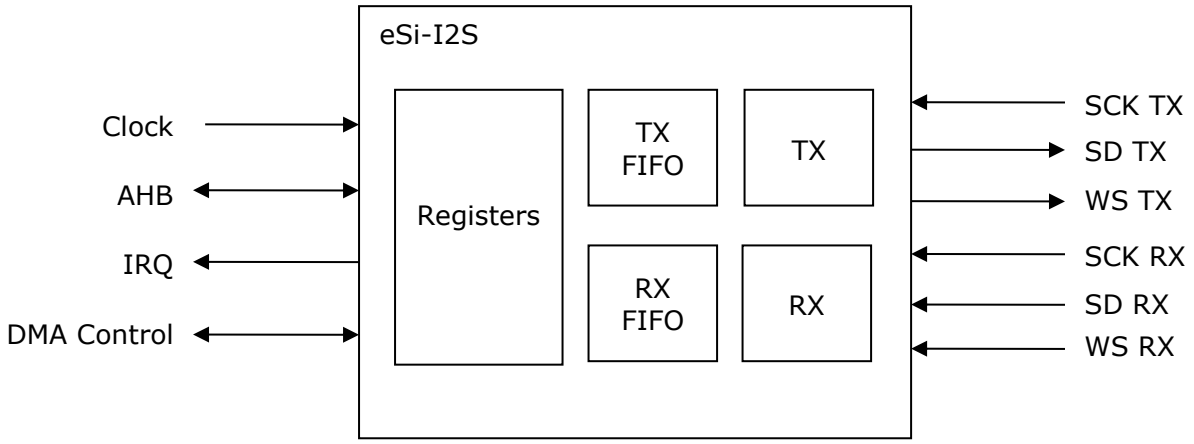


Figure 1: eSi-I2S

3 Hardware Interface

Module Name	cpu_ahb_i2s
HDL	Verilog
Technology	Generic
Source Files	cpu_ahb_i2s.v, cpu_i2s_tx.v, cpu_i2s_rx.v, cpu_peripheral_flow_control.v, cpu_async_fifo.v, cpu_reset_sync.v

Port	Type	Description
tx_fifo_depth	Integer	Specifies the depth of the TX FIFO
rx_fifo_depth	Integer	Specifies the depth of the RX FIFO

Table 1: Parameters

Port	Direction	Width	Description
scan_mode	Input	1	Indicates when in scan test mode and causes scan_reset_n to be muxed in to internal resets
scan_reset_n	Input	1	Reset to use when in scan_mode is asserted
hclk	Input	1	AHB clock
hresetn	Input	1	AHB reset, active-low
haddr	Input	BITS	AHB address
hburst	Input	3	AHB burst type
hmastlock	Input	1	AHB locked transfer
hprot	Input	4	AHB protection
hsize	Input	3	AHB size
htrans	Input	2	AHB transfer type
hwdata	Input	BITS	AHB write data
hwrite	Input	1	AHB write
hready	Input	1	AHB ready
hsel	Input	1	AHB select
sck_tx	Input	1	Serial clock for transmit interface
sck_rx	Input	1	Serial clock for receive interface
sd_rx	Input	1	Receive serial data
ws_rx	Input	1	Receive word select
tx_ack	Input	1	Acknowledges tx_ready after transfer complete
rx_ack	Input	1	Acknowledges rx_ready after transfer complete
interrupt_n	Output	1	Interrupt request, active-low
hready	Output	1	AHB ready
hrdata	Output	BITS	AHB read data
hresp	Output	1	AHB response
sd_tx	Output	1	Transmit serial data
ws_tx	Output	1	Transmit word select
tx_ready	Output	1	Indicates device can accept new data
rx_ready	Output	1	Indicates device has data to be read

Table 2: I/O Ports

For complete details of the AHB signals, please refer to the AMBA 3 AHB-Lite Protocol v1.0 Specification available at:

http://www.arm.com/products/system-ip/amba/amba-open-specifications.php

For details of the I²S bus specification, please see:

http://www.classic.nxp.com/acrobat_download2/various/I2SBUS.pdf

4 Software Interface

4.1 Register Map

Register	Address offset	Access	Description
tx_data	0x00	W	Transmit data register
rx_data	0x04	R	Receive data register
status	0x08	R/W	Status register
control	0x0c	R/W	Control register
bits_per_word	0x10	R/W	Bits per word register
txae_thresh	0x14	R/W	Transmit FIFO almost empty threshold
rxaf_thresh	0x18	R/W	Receive FIFO almost full threshold

Table 3: Register Map

4.1.1 Transmit Data Register

Data to be transmitted over the I²S interface should be written to the transmit register. The transmit data register should not be written to while the TXF bit in the status register is set, otherwise data loss may occur.

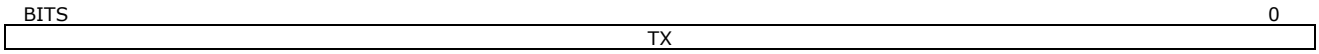


Figure 2: Format of the tx_data register

4.1.2 Receive Data Register

Data that is received over the I²S interface can be read in the receive register.

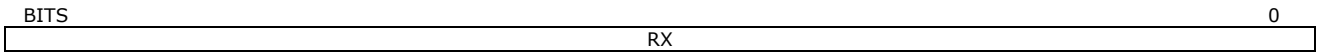


Figure 3: Format of the rx_data register

4.1.3 Status Register

The status register contains a selection of flags that indicate the current status of the I2S core. To clear a bit in the status register, write a 1 to it. Writing 0 will leave it unchanged.

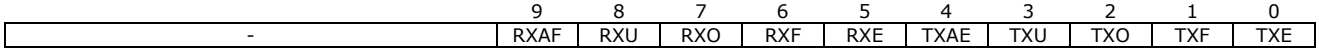


Figure 4: Format of the status register

Register	Values	Description
TXE	0 - Not empty 1 - Empty	Transmit FIFO empty
TXF	0 - Not full 1 - Full	Transmit FIFO full
TXO	0 - No overflow 1 - Overflow	Transmit FIFO overflow
TXU	0 - No underrun 1 – Underrun	Transmit FIFO underrun

TXAE	0 – Not almost empty 1 – Almost empty	Transmit FIFO almost empty
RXE	0 - Not empty 1 - Empty	Receive FIFO empty
RXF	0 - Not full 1 - Full	Receive FIFO full
RXO	0 - No overflow 1 - Overflow	Receive FIFO overflow
RXU	0 - No underrun 1 – Underrun	Receive FIFO underrun
RXAF	0 – Not almost full 1 – Almost full	Receive FIFO almost full

Table 4: Fields of the `status` register

4.1.4 Control Register

The control register contains a selection of flags that control the operation of the I2S core.

7	6	5	4	3	2	1	0
-	RXEI	TXEI	RXIE	TXIE	RXF	TXF	RXE	TXE

Figure 5: Format of the `control` register

Register	Values	Description
TXE	0 - Disabled 1 - Enabled	Enables the transmit interface
RXE	0 - Disabled 1 - Enabled	Enables the receive interface
TXF	0 – Do not flush FIFO 1 – Flush FIFO	Flushes (clears) the transmit FIFO
RXF	0 – Do not flush FIFO 1 – Flush FIFO	Flushes (clears) the receive FIFO
TXIE	0 - Disabled 1 - Enabled	Transmit interrupt enable
RXIE	0 - Disabled 1 - Enabled	Receive interrupt enable
TXEI	0 - Disabled 1 - Enabled	Transmit error interrupt enable
RXEI	0 - Disabled 1 - Enabled	Receive error interrupt enable

Table 5: Fields of the `control` register

4.1.5 Bits Per Word Register

The bits per word register specifies the number of bits in each I²S word. This can be set indecently for transmit and receive.

13	8	7	6	5	0
-	RX	-	TX

Figure 6: Format of the `bits_per_word` register

Register	Values	Description
TX	8, 16, 20, 24, 32	Number of bits per transmitted I²S word

RX	8, 16, 20, 24, 32	Number of bits per received I²S word

Table 6: Fields of the `bits_per_word` register

4.1.6 Transmit FIFO Almost Empty Threshold Register

The transmit FIFO almost empty threshold register sets the count of used entries in the transmit FIFO, below which, the `status.TXAE` flag will be set.

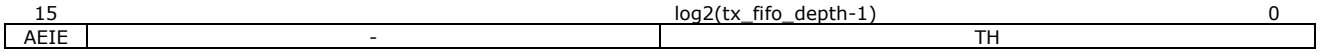


Figure 7: Format of the `txae_thresh` register

Register	Values	Description
TH	0 – `rx_fifo_size-1`	Almost empty threshold
AEIE	0 – Interrupt disabled 1 – Interrupt enabled	Almost empty interrupt enable

Table 7: Fields of the `txae_thresh` register

4.1.7 Receive FIFO Almost Full Threshold Register

The receive FIFO almost full threshold register sets the count of used entries in the receive FIFO, above which, the `status.RXAF` flag will be set.

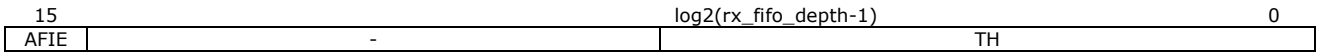


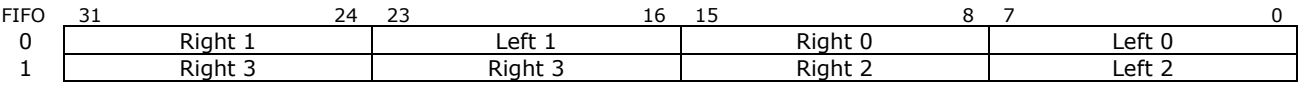
Figure 8: Format of the `rxaf_thresh` register

Register	Values	Description
TH	0 – `rx_fifo_size-1`	Almost full threshold
AFIE	0 – Interrupt disabled 1 – Interrupt enabled	Almost full interrupt enable

Table 8: Fields of the `rxaf_thresh` register

4.2 FIFO Data Format

The format of the data in the TX and RX FIFOs is determined by the `bits_per_word` register. This register specifies the number of bits per I²S word. It can be set to independent values for both TX and RX. The data is packed into the FIFO so that is word left-aligned. For example, if `bits_per_word.TX` equals 16, each 32-bit entry in the TX FIFO will contain two 16-bit words, one for the left channel and the other for the right channel. If `bits_per_word.TX` is greater than 16, each 32-bit entry in the TX FIFO will contain a single left-aligned word.



N	Right 2N+1	Right 2N+1	Right 2N	Left 2N

Table 9: FIFO Data Format when `bits_per_word.TX` equals 8

FIFO	31 16	15 0
0	Right 0	Left 0
1	Right 1	Left 1
N	Right N	Left N

Table 10: FIFO Data Format when `bits_per_word.TX` equals 16

FIFO	31 8	7 0
0	Left 0	-
1	Right 0	-
2	Left 1	-
3	Right 1	-

Table 11: FIFO Data Format when `bits_per_word.TX` equals 24

4.3 Interrupts

The I2S core supports the following interrupts.

- Transmit FIFO empty interrupt
- Transmit FIFO almost empty interrupt
- Receive FIFO full interrupt
- Receive FIFO almost full interrupt
- Transmit error interrupt
- Receive error interrupt

The transmit FIFO empty interrupt will be raised when the transmit FIFO empty flag (`TXE`) is set and the `TXIE` flag in the `control` register is set to 1. This indicates that the transmitter as run out of data to transmit.

The transmit FIFO almost empty interrupt will be raised when the transmit FIFO is almost empty as determined by `tx_thresh.TH` and the `AEIE` flag in the `tx_thresh` register is set to 1.

The receive FIFO full interrupt will be raised when the receiver FIFO full flag (`RXF`) is set and the `RXIE` flag in the control register is set to 1. This indicates that the receiver has received some data and the FIFO is full.

The receive FIFO almost full interrupt will be raised when the receive FIFO is almost full as determined by `rx_thresh.TH` and the `AFIE` flag in the `rx_thresh` register is set to 1.

The transmit error interrupt will be raised when either the transmit overflow flag (`TXO`) or transmit underrun flag (`TXU`) is set and the `TXEI` flag in the `control` register is set to 1. This indicates data loss in the transmit interface.

The receive error interrupt will be raised when either the receive overflow flag (`RXO`) or receive underrun flag (`RXU`) is set and the `RXEI` flag in the `control` register is set to 1. This indicates data loss in the receive interface.

5 Revision History

Hardware Revision	Software Release	Description
1	2.6.9	Initial release
2	3.11.12	Added `txae_thresh` register. Added `rxaf_thresh` register.

Table 12: Revision History

