eSi-RISC

PROCESSOR IP

eSi-FIFO

1 Contents

2 Overview

The eSi-FIFO core can be used to implement a FIFO between two AHB buses or masters. Its main features are:

- Configurable FIFO width and depth.
- Programmable almost full and almost empty interrupts.
- Overflow and underflow protection.
- Dual AMBA 3 AHB-lite slave interface for FIFO and control register access.

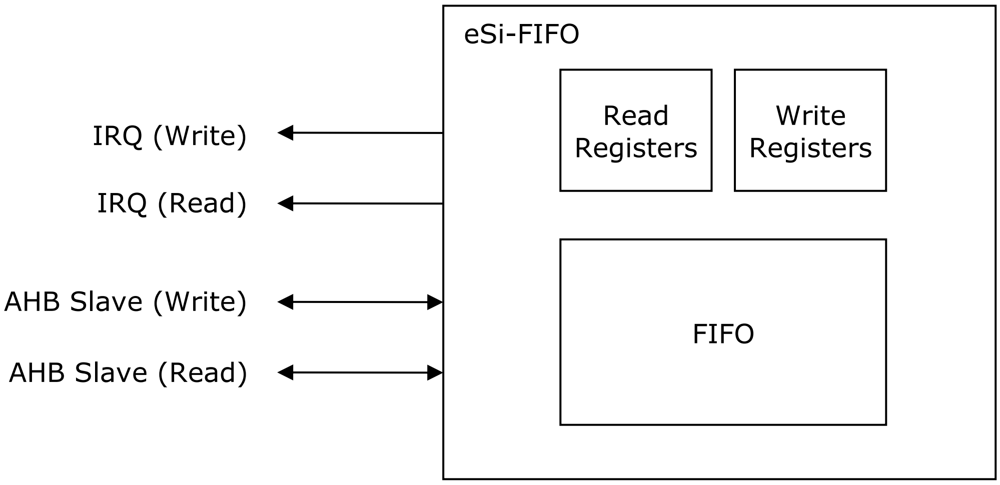

Figure 1: eSi-FIFO

3 Hardware Interface

Module Name	cpu_ahb_fifo
HDL	Verilog
Technology	Generic
Source Files	cpu_ahb_fifo.v, cpu_fifo_with_count.v

Port	Type	Description
fifo_width	Integer	Specifies the width of the FIFO
fifo_depth	Integer	Specifies the depth of the FIFO. Must be greater than 1.

Table 1: Parameters

Port	Direction	Width	Description
r_hclk	Input	1	Read slave interface, AHB clock
r_hresetn	Input	1	Read slave interface, AHB reset, active-low
r_haddr	Input	BITS	Read slave interface, AHB address
r_hburst	Input	3	Read slave interface, AHB burst type
r_hmastlock	Input	1	Read slave interface, AHB locked transfer
r_hprot	Input	4	Read slave interface, AHB protection
r_hsize	Input	3	Read slave interface, AHB size
r_htrans	Input	2	Read slave interface, AHB transfer type
r_hwdata	Input	BITS	Read slave interface, AHB write data
r_hwrite	Input	1	Read slave interface, AHB write
r_hready	Input	1	Read slave interface, AHB ready
r_hsel	Input	1	Read slave interface, AHB select
r_hready	Output	1	Read slave interface, AHB ready
r_hrdata	Output	BITS	Read slave interface, AHB read data
r_hresp	Output	1	Read slave interface, AHB response
w_hclk	Input	1	Write slave interface, AHB clock
w_hresetn	Input	1	Write slave interface, AHB reset, active-low
w_haddr	Input	BITS	Write slave interface, AHB address
w_hburst	Input	3	Write slave interface, AHB burst type
w_hmastlock	Input	1	Write slave interface, AHB locked transfer
w_hprot	Input	4	Write slave interface, AHB protection
w_hsize	Input	3	Write slave interface, AHB size
w_htrans	Input	2	Write slave interface, AHB transfer type
w_hwdata	Input	BITS	Write slave interface, AHB write data
w_hwrite	Input	1	Write slave interface, AHB write
w_hready	Input	1	Write slave interface, AHB ready
w_hsel	Input	1	Write slave interface, AHB select
w_hready	Output	1	Write slave interface, AHB ready
w_hrdata	Output	BITS	Write slave interface, AHB read data
w_hresp	Output	1	Write slave interface, AHB response
w_hclk_cactive	Output	1	Write clock active
r_interrupt_n	Output	1	Read interface interrupt request, active-low
w_interrupt_n	Output	1	Write interface interrupt request, active-low

Table 2: I/O Ports

For complete details of the AHB signals, please refer to the AMBA 3 AHB-Lite Protocol v1.0 Specification available at:

http://www.arm.com/products/system-ip/amba/amba-open-specifications.php

4 Software Interface

4.1 Register Map

Both the read and write AHB slave interfaces have their own set of the following registers:

Register	Address offset	Access	Description
data	0x00	R/W	Data register
status	0x04	R/W	Status register
control	0x08	R/W	Control register
ae_thresh	0x0c	R/W	FIFO almost empty threshold
af_thresh	0x10	R/W	FIFO almost full threshold
count	0x14	R	Count register
max_count	0x18	R/W	Max count register

Table 3: Register Map

4.1.1 Data Register

The data register can be written in order to write data to the FIFO and can be read in order to read data from the FIFO. Attempting to write the FIFO from the read AHB interface will result in an error, as will reading from the write AHB interface.

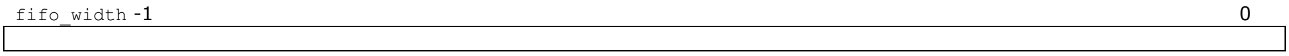

Figure 2: Format of the data register

4.1.2 Status Register

The status register contains a selection of flags that indicate the current status of the FIFO. The E, F, NE, AE and AF flags are read only. The O and U flags are sticky. To clear the O or U flag, write a 1 to it. Writing 0 will leave it unchanged.

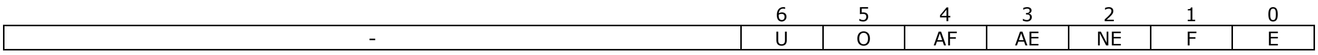

Figure 3: Format of the status register

Register	Values	Description
E	0 – Not empty 1 – Empty	FIFO empty
F	0 – Not full 1 – Full	FIFO full
NE	0 – Empty 1 – Not empty	FIFO not empty
AE	0 – Not almost empty 1 – Almost empty	FIFO almost empty
AF	0 – Not almost full 1 – Almost full	FIFO almost full
O	0 – No overflow 1 – Overflow	FIFO overflow (write when full)
U	0 – No underflow 1 – Underflow	FIFO underflow (read when empty)

Table 4: Fields of the `status` register

4.1.3 Control Register

The control register contains a selection of flags that control the operation of the FIFO.

	9	8	7	6	5	4	3	2	1	0
	DR	DW	-	UIE	OIE	AFIE	AEIE	NEIE	FIE	EIE

Figure 4: Format of the `control` register

Register	Values	Description
`EIE`	0 – Interrupt disabled 1 – Interrupt enabled	Empty interrupt enable
`FIE`	0 – Interrupt disabled 1 – Interrupt enabled	Full interrupt enable
`NEIE`	0 – Interrupt disabled 1 – Interrupt enabled	Not empty interrupt enable
`AEIE`	0 – Interrupt disabled 1 – Interrupt enabled	Almost empty interrupt enable
`AFIE`	0 – Interrupt disabled 1 – Interrupt enabled	Almost full interrupt enable
`OIE`	0 – Interrupt disabled 1 – Interrupt enabled	Overflow interrupt enable
`UIE`	0 – Interrupt disabled 1 – Interrupt enabled	Underflow interrupt enable
`DW`	0 – Allow overflow 1 – Delay write	Deassert AHB `w_hready` on write to full FIFO. This should be used carefully as the bus can become deadlocked, depending upon bus architecture
`DR`	0 – Allow underflow 1 – Delay read	Deassert AHB `r_hready` on read from empty FIFO. This should be used carefully as the bus can become deadlocked, depending upon bus architecture

Table 5: Fields of the `control` register

4.1.4 Almost Empty Threshold Register

The almost empty threshold register sets the count of used entries in the FIFO, below which, the `status.AE` flag will be set.

15	log2(fifo_depth) 0
-	TH

Figure 5: Format of the `ae_thresh` register

Register	Values	Description
`TH`	0 – `fifo_depth`	Almost empty threshold

Table 6: Fields of the `ae_thresh` register

4.1.5 Almost Full Threshold Register

The almost full threshold register sets the count of used entries in the FIFO, above which, the `status.AF` flag will be set.

15	log2(fifo_depth) 0
-	TH

Figure 6: Format of the `af_thresh` register

Register	Values	Description
TH	0 – fifo_depth	Almost full threshold

Table 7: Fields of the `af_thresh` register

4.1.6 Count Register

The `count` register indicates the count of used entries in the FIFO.

	log2(fifo_depth) 0
-	C

Figure 7: Format of the `count` register

Register	Values	Description
C	0 – fifo_depth	Count of used entries in FIFO

Table 8: Fields of the `count` register

4.1.7 Max Count Register

The `max_count` register indicates the maximum count of used entries in the FIFO. Writing to this register will reset it to 0.

	log2(fifo_depth) 0
-	MC

Figure 8: Format of the `count` register

Register	Values	Description
MC	0 – fifo_depth	Maximum count of used entries in FIFO

Table 9: Fields of the `max_count` register

4.2 Interrupts

The FIFO supports the following interrupts:

- FIFO full
- FIFO almost full
- FIFO empty
- FIFO almost empty

- FIFO not empty
- FIFO overflow
- FIFO underflow

5 Revision History

Hardware Revision	Software Release	Description
1	3.3.0	Initial release
2	4.0.3	Add `control.DR` and `control.DW`

Table 10: Revision History