eSi-CPU-to-CPU Interrupt

1   Contents

2   Overview

The eSi-CPU-to-CPU Interrupt core provides a simple way to generate CPU-to-CPU interrupts in a system where each CPU is connected to a shared AHB. It supports the following features:

- Configurable number of interrupt pins (1-32).
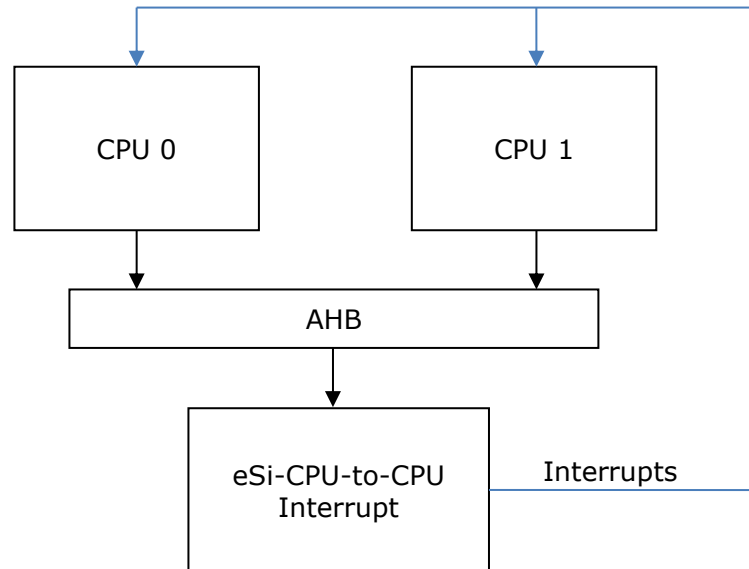- AMBA 3 AHB-lite slave interface.

Figure 1: eSi-CPU-to-CPU Interrupt System Example

3   Hardware Interface

Module Name	cpu_ahb_cpu_to_cpu_interrupt
HDL	Verilog
Technology	Generic
Source Files	cpu_ahb_cpu_to_cpu_interrupt.v

Port	Type	Values	Description
interrupts	Integer	1-32	Specifies the width of the interrupt_n bus

Table 1: Parameters

Port	Direction	Width	Description
hclk	Input	1	AHB clock
hresetn	Input	1	AHB reset, active-low
haddr	Input	BITS	AHB address
hburst	Input	3	AHB burst type
hmastlock	Input	1	AHB locked transfer
hprot	Input	4	AHB protection
hsize	Input	3	AHB size
htrans	Input	2	AHB transfer type
hwdata	Input	BITS	AHB write data
hwrite	Input	1	AHB write
hready	Input	1	AHB ready
hsel	Input	1	AHB select
hready	Output	1	AHB ready
hrdata	Output	BITS	AHB read data
hresp	Output	1	AHB response
interrupt_n	Output	interrupts	Interrupts, active-low

Table 2: I/O Ports

For complete details of the APB signals, please refer to the AMBA 3 APB Protocol v1.0 Specification available at:

http://www.arm.com/products/system-ip/amba/amba-open-specifications.php

4 Software Interface

4.1 Register Map

Each interrupt has a pair of control registers, as illustrated in Table 3: Register Map. In this table, `N` indicates the interrupt, which ranges from 0 to `interrupts`-1.

Register	Address offset	Access	Description
control[N]	0x10*N+0x00	R/W	Interrupt control register
acknowledge[N]	0x10*N+0x04	W	Interrupt acknowledge register

Table 3: Register Map

4.1.1 Control Register

The per-interrupt control register controls whether the corresponding interrupt is enabled. The control register should only be written by the CPU that is the source of the interrupt.
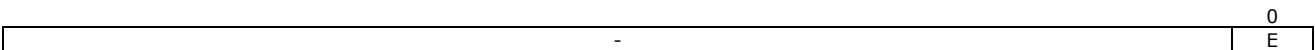
	0
-	E

Figure 2: Format of the `control` register

Register	Values	Description
E	0 – Disabled 1 – Enabled	Interrupt enable

Table 4: Fields of the `control` register

4.1.2 Acknowledge Register

The per-interrupt acknowledge register can be used to acknowledge the corresponding interrupt. This clears the corresponding enable bit in the control register.
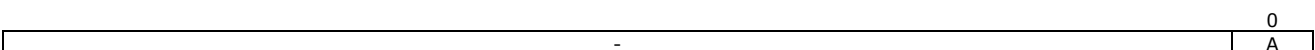
	0
-	A

Figure 3: Format of the `acknowledge` register

Register	Values	Description
A	0 – Do not acknowledge 1 – Acknowledge	Interrupt acknowledge

Table 5: Fields of the `acknowledge` register

5   Revision History

Hardware Revision	Software Release	Description
1	2.4.0	Initial release

Table 6: Revision History