

## Application Areas

- ▶ DVB-T(2), DVB-S(2)
- ▶ 802.11a/n
- ▶ 802.16
- ▶ HomePlugAV

## Features

- ▶ Slices BPSK, QPSK, 16-QAM, 64-QAM, 256-QAM and 1024-QAM
- ▶ Generates Log Likelihood Ratio bit metrics
- ▶ Produces up to 10 LLR bit-metrics per clock
- ▶ Capable of sustained 1.5G LLRs/sec
- ▶ Supports adaptive bit loading

## Specification

This is a high throughput QAM constellation demapper and Log Likelihood Ratio (LLR) bit-metric generator. The core is capable of accepting a new equalised QAM symbol per clock cycle and generates all the bit-metrics for that symbol after a short latency. The subcarrier QAM modulation is specified each clock cycle to accommodate systems supporting adaptive bit loading. The QAM channel state information (CSI) can be specified on the same clock cycle as the QAM symbol to allow the LLR to be correctly weighted.

The QAM symbol is quantised to 12-bits covering the range +/-2.0 on both I and Q for a typical equalised constellation. The CSI is a linear signal-to-noise ratio in the range 0.25 to 8191, which spans -6dB to +40dB.

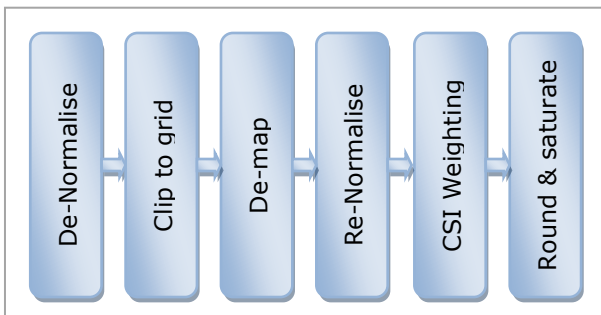


Figure 1: Block diagram

The first stage is to map the normalised constellation points to the conventional QAM grid for that modulation format. This involves multiplying by  $1/K_{mod}$ , where  $1/K_{mod}^2$  is the constellation energy. These resulting grids are bounded by  $\{+/-2, +/-2, +/-4, +/-8, +/-16, +/-32\}$  for BPSK to 1024-QAM respectively. This is referred to as de-normalization and would return the QAM symbols to the QAM grid centres in the absence of noise.

The next stage clips any points outside the grid to the grid edges avoiding noise amplification.

Following this all operations apply on the bit-metrics and determine for each of them the difference of squared distances from the constellation point to its nearest hard decision "1" or "0" in that bit position. The constellation is assumed to be Gray coded for this operation.

The difference of squared distances are re-normalised by  $K_{mod}^2/4$ , so each modulation format has the same range. The renormalised difference of squared distances are weighted by the CSI and finally rounded and saturated to an LLR range of +/-8.0 in steps of 0.25, i.e. 6 bits. This provides excellent soft decision information for subsequent forward error correction, for example Viterbi, Turbo or LDPC.

## Benefits

The EnSilica QAM demodulator implementation is efficient and flexible; suitable for both ASIC and FPGA implementation. It benefits from a simple pipelined dataflow structure to allow easy interfacing to the rest of the system. This decoder achieves an OFDM throughput of 150M subcarriers/sec or 1.5G LLRs/sec. The exceptional internal precision means that high order QAM constellations are accurately sliced and sufficient soft information is retained even for the least well protected bits.

## Resources

The following represent typical logic and memory resources are for an Altera Cyclone III. Specifying a maximum order less than 1024-QAM significantly reduces the logic and multipliers.

Variant	Logic LUTs	M9K	9-bit mul	Fmax MHz
12-bit QAM 16-bit CSI <=1024-QAM	1700	2	44	150

## About EnSilica

EnSilica is an established company with many years experience providing high quality IC design services to customers undertaking FPGA and ASIC designs. We have an impressive record of success working across many market segments with particular expertise in multimedia and communication applications. Our customers range from start-ups to blue-chip companies. EnSilica can provide the full range of front-end IC design services, from System Level Design, RTL coding and Verification through to either a FPGA device or the physical design interface (synthesis, STA and DFT) for ASIC designs. EnSilica also offer a portfolio of IP, including a highly configurable 16/32 bit embedded processor called eSi-RISC and the eSi-Comms range of communications IP.

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