

Application Areas

- ▶ DVB using (204, 188)
- ▶ G.975/G.709 using (255, 239)
- ▶ CCDS using (255, 223)
- ▶ DSL
- ▶ 802.16-2004 WiMax using (255, 239)

Features

- ▶ Based on standard RS generating polynomials 285_8 or 207_8 .
- ▶ Available for FPGA or ASIC
- ▶ Supports shortening
- ▶ Supports erasures

Specification

The RS encoder is based on a (255, 239) / (255, 223) block encoding, so there are 16/32 parity bytes in the resulting codeword respectively. This coding provides correction for up to 8/16 bytes of data anywhere in the codeword. No parity bytes are erased. A shortened message is one where the message and codeword length are less than the full block length, but must still obey the rule that the codeword has 16/32 more bytes than the message. So for instance a rate 1/2 encoder can be formed from a message of 16/32 bytes, to which 16/32 parity bytes are added. Shortened messages are ones for which the leading bytes are all zero, and can be quickly encoded by starting the remainder from zero for the first message byte.

The encoding is performed by a circuit consisting of a 16/32 stage shift register of bytes that hold the remainder of the input message divided by the field polynomial. The remainder after all the message bytes have been processed is known as the parity. The division is over a Galois field of 8 bit messages having generator polynomial 285_8 or 207_8 . The encoding is systematic so that the input bytes are passed through, followed by the 16/32 parity bytes. The GF multipliers are implemented as binary multipliers reduced modulo the generator polynomial.

The IP has a bypass mode to continue passing any pad bytes to the next stage.

The encoder can process one input byte per 2 clock cycles. It will output a parity byte per 2 clock cycles following the last message byte. This implies a maximum throughput rate of $4 \times \text{CLK}$ bps.

In bypass mode it will pass one byte per clock cycle with a 1 cycle delay for double buffering to allow flow control.

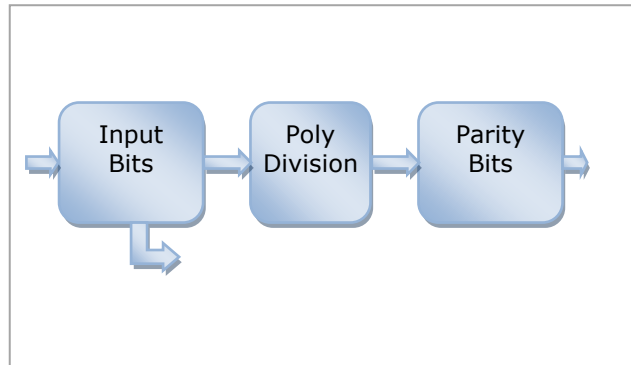


Figure 1: Block diagram

Resources

The following represent typical logic and memory resources are for an Altera Cyclone III.

Variant	Logic LUT	Memory (Bits)	Fmax MHz
G.709	200	0	200

About EnSilica

EnSilica is an established company with many years experience providing high quality IC design services to customers undertaking FPGA and ASIC designs. We have an impressive record of success working across many market segments with particular expertise in multimedia and communication applications. Our customers range from start-ups to blue-chip companies. EnSilica can provide the full range of front-end IC design services, from System Level Design, RTL coding and Verification through to either a FPGA device or the physical design interface (synthesis, STA and DFT) for ASIC designs. EnSilica also offer a portfolio of IP, including a highly configurable 16/32 bit embedded processor called eSi-RISC and the eSi-Comms range of communications IP.

www.ensilica.com