eSi-UART

1 Contents

2 Overview

The eSi-UART core can be used to implement asynchronous serial communications. It supports the following features:

- 7 or 8 data bits.
- 1 or 2 stop bits.
- Parity bit (None / Even / Odd / Mark / Space).
- Optional RTS/CTS flow control.
- Programmable bit rate.
- ISO 7816-3 T=0 and T=1 support, with NACK and retry.
- Configurable RX FIFO.
- AMBA 3 APB slave interface.
- DMA flow-control interface.

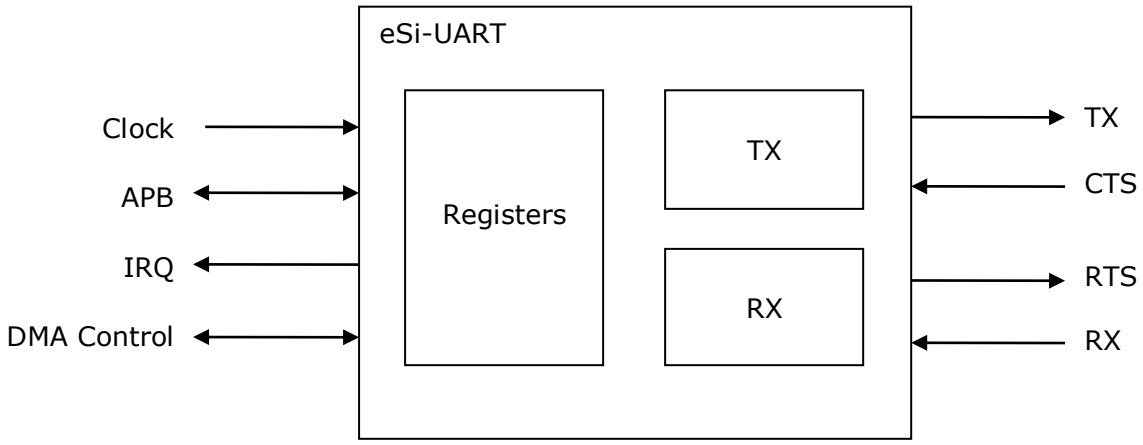

Figure 1: eSi-UART

3 Hardware Interface

Module Name	cpu_apb_uart
HDL	Verilog
Technology	Generic
Source Files	cpu_apb_uart.v, cpu_fifo.v, cpu_peripheral_flow_control.v

Port	Type	Description
default_cycles_per_bit	Integer	Specifies the reset value of the cycles_per_bit register
rx_fifo_depth	Integer	Specifies the depth of the RX FIFO

Table 1: Parameters

Port	Direction	Width	Description
clk	Input	1	Clock used for serial data transmission and reception. This clock must be enabled when cactive is asserted. This clock will be divided by the value in the cycles_per_bit register. This clock must be the same frequency and synchronouns to pclk.
pclk	Input	1	APB clock
presetn	Input	1	APB reset, active-low
paddr	Input	8	APB address
psel	Input	1	APB slave select
penable	Input	1	APB enable
pwrite	Input	1	APB write
pwdata	Input	16	APB write data
rx	Input	1	Receive data
cts_n	Input	1	Clear to send, active-low
tx_ack	Input	1	Acknowledges tx_ready after transfer complete
rx_ack	Input	1	Acknowledges rx_ready after transfer complete
cactive	Output	1	Clock active
pready	Output	1	APB ready
prdata	Output	16	APB read data
pslverr	Output	1	APB slave error
tx	Output	1	Transmit data
rts_n	Output	1	Ready to send, active-low
duplex	Output	1	Indicates full duplex (0) or half-duplex (1) operation
interrupt_n	Output	1	Interrupt request, active-low
tx_ready	Output	1	Indicates device can accept new data
rx_ready	Output	1	Indicates device has data to be read

Table 2: I/O Ports

For complete details of the APB signals, please refer to the AMBA 3 APB Protocol v1.0 Specification available at http://www.arm.com/products/solutions/AMBAHomePage.html

The UART does not include internal synchronizing flip-flops. These should be implemented externally for the rx and cts_n ports if the transmitting clock domain is asynchronous to clk.

4 Software Interface

4.1 Register Map

Register	Address offset	Access	Description
tx_data	0x00	W	Transmit data register
rx_data	0x04	R	Receive data register
status	0x08	R/W	Status register
control	0x0c	R/W	Control register
cycles_per_bit	0x10	R/W	Cycles per bit register
retries	0x14	R/W	Retries register

Table 3: Register Map

4.1.1 Transmit Data Register

Data to be transmitted over the serial interface should be written to the lower 8 bits of the transmit data register. The transmit data register should not be written to while the TXF bit in the status register is set, otherwise data loss may occur.

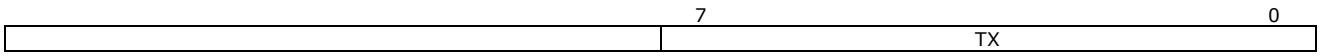

Figure 2: Format of the tx_data register

4.1.2 Receive Data Register

Data that is received over the serial interface can be read in the lower 8 bits of the receive data register.

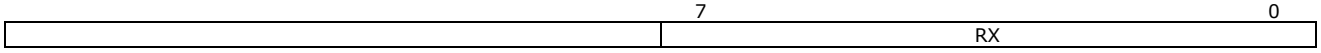

Figure 3: Format of the rx_data register

4.1.3 Status Register

The status register contains a selection of flags that indicate the current status of the UART. To clear a bit in the status register, write a 1 to it. Writing 0 will leave it unchanged.

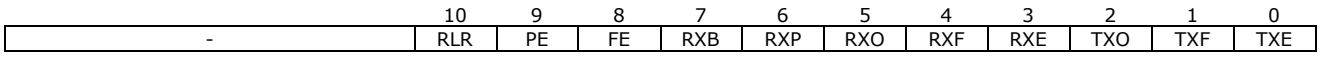

Figure 4: Format of the status register

Register	Values	Description
TXE	0 - Not empty 1 - Empty	Transmit buffer empty
TXF	0 - Not full 1 - Full	Transmit buffer full
TXO	0 - No overflow 1 - Overflow	Transmit buffer overflow
RXE	0 - Not empty 1 - Empty	Receive buffer empty

RXF	0 - Not full 1 - Full	Receive buffer full
RXO	0 - No overflow 1 - Overflow	Receive buffer overflow
RXP	0 - Parity bit was 0 1 - Parity bit was 1	Received parity bit
RXB	0 - Break not received 1 - Break received	Received break
FE	0 - No error 1 - Framing error	Framing error
PE	0 - No error 1 - Parity error	Parity error
RLR	0 – Not reached 1 – Reached	Retry limited reached

Table 4: Fields of the `status` register

4.1.4 Control Register

The control register contains a selection of flags that control the operation of the UART.

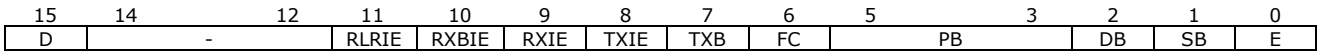

Figure 5: Format of the `control` register

Register	Values	Description
E	0 - Disabled 1 - Enabled	Enables the UART. When disabled, data will not be received or transmitted
SB	0 - 1 stop bit 1 - 2 stop bits	Number of stop bits
DB	0 - 8 data bits 1 - 7 data bits	Number of data bits
PB	0 - No parity bit 1 - Even parity 2 - Odd parity 3 - Mark 4 - Space 5 – ISO 7816-3 T=0	Parity bit
FC	0 - No flow control 1 - RTS/CTS	Flow control
TXB	0 - Do not send break 1 - Send break	Transmit break. When set, the transmit data line will be held low, signalling a break
TXIE	0 - Disabled 1 - Enabled	Transmit interrupt enable
RXIE	0 - Disabled 1 - Enabled	Receive interrupt enable
RXBIE	0 - Disabled 1 - Enabled	Receive break interrupt enable
RLRIE	0 – Disabled 1 – Enabled	Retry limited reached interrupt enabled
D	0 – Full duplex 1 – Half duplex	Duplex

Table 5: Fields of the `control` register

4.1.5 Cycles Per Bit Register

The cycles per bit register is a 16-bit that specifies how many cycles of the clock, `clk`, each bit is transmitted for. Use of a 16-bit register provides support for a wide range of clock frequencies and baud rates.

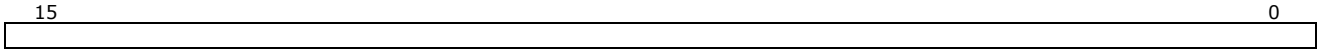

Figure 6: Format of the `cycles_per_bit` register

4.1.6 Retries Register

The retries register holds a 3-bit unsigned integer that specifies how many times the UART should attempt retransmission of a character, when a parity error is signalled. Retransmission is only enabled when `control.PB` equals 5 (ISO 7816-3 T=0).

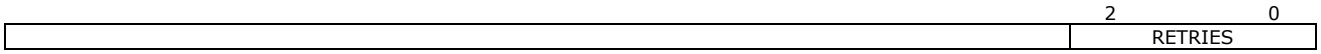

Figure 7: Format of the `retries` register

4.2 Interrupts

The UART supports the following interrupts.

- Transmit interrupt
- Receive interrupt
- Break interrupt
- Retry limit reached interrupt

The transmit interrupt will be raised when the transmit buffer is empty and the `TXIE` flag in the `control` register is set to 1. This indicates that the transmitter has no data to transmit.

The receive interrupt will be raised when the receiver buffer is not empty and the `RXIE` flag in the control register is set to 1. This indicates that the receiver has received some data.

The break interrupt will be raised then a break is detected on the receive data line and the `RXBIE` flag in the `control` register is 1. This interrupt can be acknowledged by writing a 1 to the `RXB` flag in the `status` register.

The retry limit reached interrupt will be raised when the parity mode is set to 5 (ISO 7816-3 T=0) and the UART has received a parity error signal for the transmission and each subsequent retransmission of a character. The number of times a character is attempted to be transmitted is determined by the `retries` register. The `RLR` flag in the `status` register will be set to 1 to indicate this limit being reached. The interrupt can be acknowledged by writing a 1 to the `RLR` flag in the `status` register.

4.3 ISO 7816-3 Operation

The eSi-UART supports both ISO 7816-3 T=0 and T=1 operation.

- For T=0 operation, the UART's `control` register should be configured as illustrated in Table 6: T=0 `control` Register Settings. The `retries` register should be set to the desired number of retries.

Field	Value	Description
E	1	Enabled
SB	1	2 stop bits
DB	0	8 data bits
PB	5	ISO 7816-3 T=0 parity
FC	0	No flow control
TXB	0	Do not send break
D	1	Half duplex

Table 6: T=0 `control` Register Settings

- For T=1 operation, the UART's control register should be configured as illustrated in Table 7: T=1 `control` Register Settings. The `retries` register should be set to 0.

Field	Value	Description
E	1	Enabled
SB	0	1 stop bits
DB	0	8 data bits
PB	1	Even parity
FC	0	No flow control
TXB	0	Do not send break
D	1	Half duplex

Table 7: T=1 `control` Register Settings

To use the eSi-UART in an ISO 7816-3 application, where communication is half-duplex over a single bi-directional line, the eSi-UART should be connected as illustrated in Figure 8: Bi-directional I/O Interfacing.

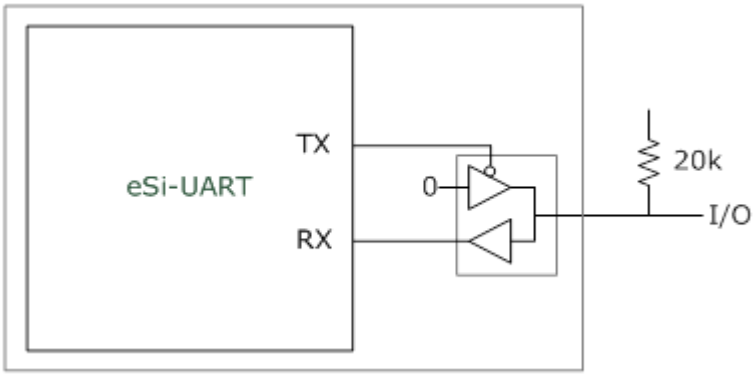

Figure 8: Bi-directional I/O Interfacing

5 Revision History

Hardware Revision	Software Release	Description
1	1.0.0	Initial release
2	2.4.0	Added ISO 7816-3 support. Added `status.RLR` register field. Added `control.PB` mode 5. Added `control.RLRIE` register field. Added `retries` register. Added retry limit reached interrupt. Added `tx_ack` and `rx_ack` ports. Added `duplex` output.

Table 8: Revision History

