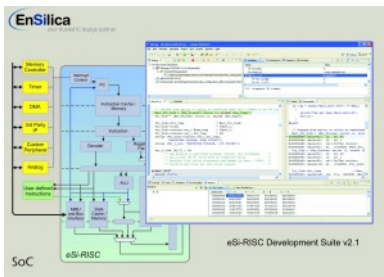


PRESS RELEASE

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EnSilica launches major new version of its eSi-RISC Development Suite

Enables the quick and simple deployment of eSi-RISC low-power configurable processor cores



Wokingham and Cambridge, UK – 29th March 2010. EnSilica, a leading independent provider of front-end IC design services, has launched a major new version of its eSi-RISC Development Suite. The eSi-RISC Development Suite v2.1 provides a comprehensive platform for easily evaluating EnSilica's family of eSi-RISC highly configurable and low-power soft processor cores, along with a complete development environment for the creation, implementation and test of eSi-RISC processor embedded application designs.

The eSi-RISC Development Suite v2.1 includes a new hardware evaluation platform based on Altera's Cyclone III FPGA with rapid software development and debugging facilitated through the Eclipse IDE (Integrated Development Environment) and industry-standard GNU GCC 4.4.0 toolchain, which now features native support for the eSi-RISC architectural features. FPGA configurations are supplied for the complete eSi-RISC processor family, along with numerous application examples demonstrating how the system-on-chip peripherals can be used, including a full port of the open source FreeRTOS with lwIP TCP/IP network stack. Comprehensive documentation and a range of interactive tutorials are also included.

Extensive debug facilities in the eSi-RISC Development Suite v2.1 also significantly enhance development productivity. Non-intrusive debugging for FPGAs is provided through the JTAG hardware debugger, which provides the ability to examine data, insert break and watchpoints and control program execution, giving developers full read/write access to all variables, registers, memory and attached peripherals, while supporting single-step and step-over execution of the C code and views of the disassembly. Debugging is seamless with communication over a USB interface to a host PC with GDB, the GNU project debugger, running inside Eclipse.

The eSi-RISC Development Suite v2.1 also allows developers to debug code using hardware/software co-simulation by enabling remote control of Mentor Graphics' ModelSim from the Eclipse GDB project debugger through a network socket connection. ModelSim conveniently displays disassembled instructions as text in the wave display which is especially helpful for SoC level hardware and software debugging.

Network application debugging is also considerably simplified with the integration of WinPcap into the new eSi-RISC Development Suite's Instruction Set Simulator to emulate the eSi-EMAC Ethernet MAC peripheral connection. This makes it possible, for instance, to run a Web Server on eSi-RISC with a live Ethernet connection serving web pages to a browser running on a remote computer.

"The ease and speed with which processors can be evaluated and applications developed and tested, plays an important role in developers' choice of processors," said Ian Lankshear, Managing Director of EnSilica. "The eSi-RISC Development Suite v2.1 includes a host of new features and capabilities to enable our eSi-RISC processor family to be easily evaluated and quickly deployed."

About the eSi-RISC processor family

eSi-RISC is a family of highly configurable and low-power soft processor cores for embedded systems that scales across a wide range of applications and uniquely supports both 16 and 32-bit configurations. The eSi-RISC family of processors has been extensively silicon proven in a number of ASIC and FPGA technologies. The eSi-RISC family includes the eSi-1600 16-bit processor, eSi-3200 32-bit processor, eSi-3250 32 bit processor and eSi-3250sfp incorporating a single precision floating point processor. The processor cores also benefit from selectable Harvard/von Neumann memory and configurable cache options. The highly pipelined nature of their design gives customers a technology-independent solution that is ideal for both FPGA applications and ASIC technologies.

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About EnSilica

EnSilica is an established company with many years experience providing high quality IC design services to customers undertaking FPGA and ASIC designs. EnSilica has an impressive record of success working across many market segments with particular expertise in multimedia and communications applications. Customers range from start-ups to blue-chip companies. EnSilica can provide the full range of front-end IC design services, from System Level Design, RTL coding and Verification through to either a FPGA device or the physical design interface (synthesis, STA, DFT) for ASIC designs. EnSilica also offers a portfolio of IP, including a highly configurable 16/32 bit embedded processor called eSi-RISC and the eSi-Comms range of communications IP. For further information about EnSilica, visit <http://www.ensilica.com>. eSi-RISC product information and downloads can be found at <http://www.esi-risc.com>.

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